Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (Currently Amended) A parallel processor comprising:

a global processor interpreting a program and controlling the entirety of the parallel processor; and

a processor-element block comprising a plurality of processor elements each comprising a register file and an operation array for processing a plurality of sets of data,

wherein said global processor assigns to said plurality of processor elements respective processor-element numbers, and outputs a control signal to said plurality of processor elements, and, thereby, sets the assigned processor-element numbers corresponding to said plurality of processor elements as input values of the operation arrays, respectively, and

~~wherein for each processor element said register file of the processor element holds plural sets of data for operation processing by the operation array of the processor element, according to processor element instructions from the global processor, and~~

~~wherein the operation array of the processor element includes a multiplexer coupled to the register file of the processor element and to the register files of respective adjacent processor elements~~

wherein said plurality of processor elements are divided into pairs of an even-numbered processor element and an odd-numbered processor element, each pair specified by a single address such that write data is transferred to one of the even-numbered processor element and the

odd-numbered processor element and read data is read from the other, by a single addressing operation.

2. (Previously Presented) The parallel processor as claimed in claim 1, wherein data from a general-purpose register of said global processor is transferred to arbitrary processor elements of said plurality of processor elements.

3. (Previously Presented) The parallel processor as claimed in claim 2, wherein the data transfer is rendered through specifying a range from a first specific processor element through a second specific processor element by specifying immediate values by using operands.

4. (Previously Presented) The parallel processor as claimed in claim 2, wherein

the data transfer is rendered through specifying bits such as to specify processor elements matching processor-element numbers expressed in binary notation; and

specifying processor elements by masking arbitrary bits of the specified bits, through specifying the immediate values by using the operands.

5. (Previously Presented) The parallel processor as claimed in claim 2, wherein the data transfer is rendered through specifying by a pointer using a general-purpose register of said global processor.

6. (Previously Presented) The parallel processor as claimed in claim 5, wherein the specifying by a pointer comprises incrementing of data in said general-purpose register after the specifying.

7. (Previously Presented) The parallel processor as claimed in claim 1, wherein each processor element comprises a plurality of flag bits for controlling, according to a state of the data, as to whether or not the operation processing is to be executed, according to whether or not a condition is satisfied, and, renders AND/OR operation on a specific bit of said flag bits.

8. (Previously Presented) The parallel processor as claimed in claim 7, wherein specifying of said flag bits is rendered by specifying the range from the first specific processor element through the second specific processor element through specifying the immediate values by using the operands.

9. (Previously Presented) The parallel processor as claimed in claim 7,

wherein specifying of said flag bits is rendered through specifying bits such as to specify processor elements matching processor-element numbers expressed in binary notation; and

specifying processor elements by masking arbitrary bits of the specified bits through specifying the immediate values by using the operands.

10. (Previously Presented) The parallel processor as claimed in claim 7, wherein specifying of said flag bits is rendered through specifying by a pointer using a general-purpose register of said global processor.

11. (Previously Presented) The parallel processor as claimed in claim 10, wherein the specifying by a pointer comprises incrementing of data in said general-purpose register after the specifying.

Claims 12-22 (Canceled).

23. (Previously Presented) The parallel processor as claimed in claim 1, wherein each processor element further includes a shift and expansion circuit.